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**TPS Activity 1**

1. Cache is a copy of a small portion of the main memory. We need the cache so that we can use small portions of data faster.
2. With 16B we need 4 bits for offset. log2(16) = 4 bits. In most cases it is not practical to have a cache of block size = 1 byte.
3. With 64 blocks in the cache we need 6 index bits. log2(64) = 6 bits.
4. With both the number of blocks and the block size we know the size of the cache because we now know the length and height of the cache. We know the number of rows and columns in the cache.
5. The left over bits from the address are used for the tag. They help tell if the information in the block is backed up or not. With this information we can back up the information that we need.
6. mem add of 20 bits, 128B cache, 8B block size
7. It is 128 Bytes big
8. There are 3 offset bits
9. There are 16 blocks in the cache
10. There are 4 index bits
11. There are 13 tag bits

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| V | D | tag | <----- | ------ | block | ------ | ----- | ----- | ----- | ----> |
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1. The cache has 80 bits per row. ((block\_size \* 8) + valid + dirty + tags)

**TPS Activity 2**

1. The disadvantage is that there will eventually be a long hit time. It will take much longer to get a hit if the cache gets large enough to have less hit misses. It will introduce a cache miss with block replacement.
2. We need
3. 20 bit mem, 128B 2-way cache, 8B block size
4. The main memory is 20 bits
5. There are 3 offset bits
6. There are 16 blocks in the cache
7. There are 4 sets in the cache
8. There are 4 index bits
9. There are 13 tag bits

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| valid | dirty | tag | <---- | ------ | ------ | block | ------ | ------ | ------ | ----> |
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1. There are 80 bits per row in the cache.

**Assignment (cache in your computer)**

1. My CPU has 3 levels of caches, L1, L2, and L3. Yes, there are separate L1 caches for data and instructions.
2. The L1 data cache is 16KB. The L1 instruction cache is 64KB. The L2 cache is 2048KB. The L3 cache is 8MB.
3. The block size for all of the caches is 64B.
4. They are set associative. L1 Data is 4-way. L1 Instruction is 2-way. L2 is 16-way. L3 is 64-way.
5. In L1 data cache there are 5 offset bits, 5 index bits, and 54 tag bits